# ReRAM Characterization Vehicle

*EE/CprE 4920 Industry Review Panel Presentation*

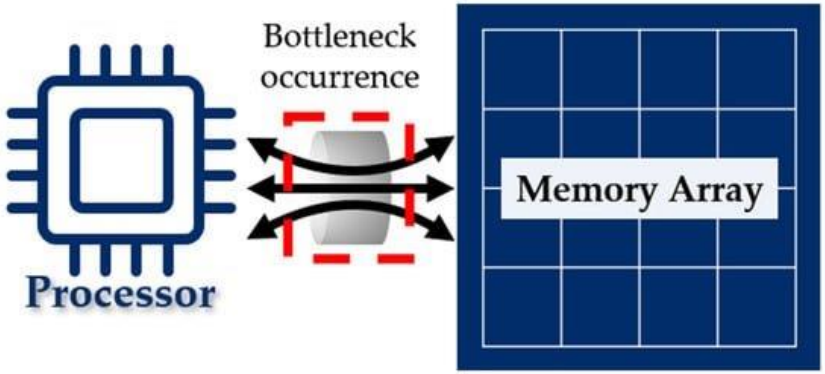
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IOWA STATE UNIVERSITY

# Introduction and Context

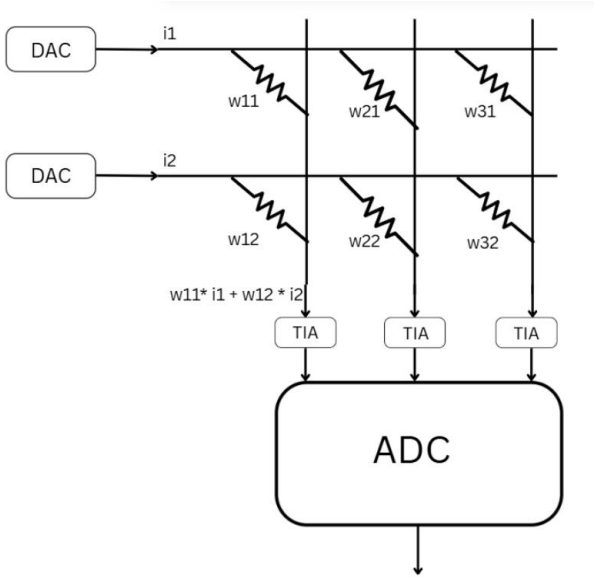
# Problem Statement

- How do computers perform calculations?
- Problems with the traditional way of computation
- Memory to processor to memory
- What if memory and the processor could do the same thing?



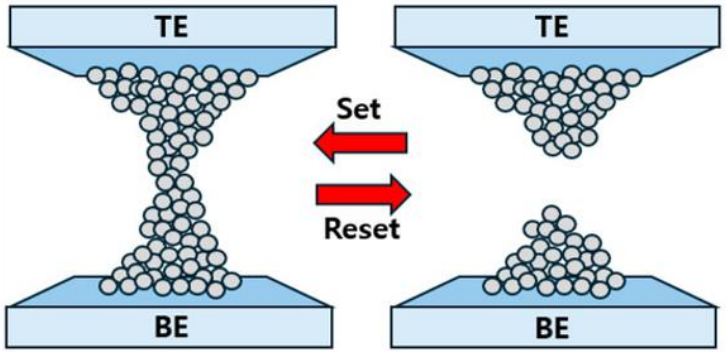
# Compute In-memory problems

- Typical Mixed-Signal IC design issues
  - Temperature dependence
- Sensitivity to noise



# ReRAM for Compute in-memory

- ReRAM is a relatively new technology
- Poorly understood behavior
- Provide researchers the ability to characterize ReRAM and its application



# Clients

- Primary client - ISU Research Staff – Prof. Cheng and his team
  - In-memory computing materials and devices
- ISU Chipforge Club

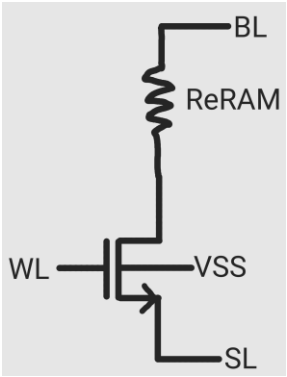
# Requirements and Constraints

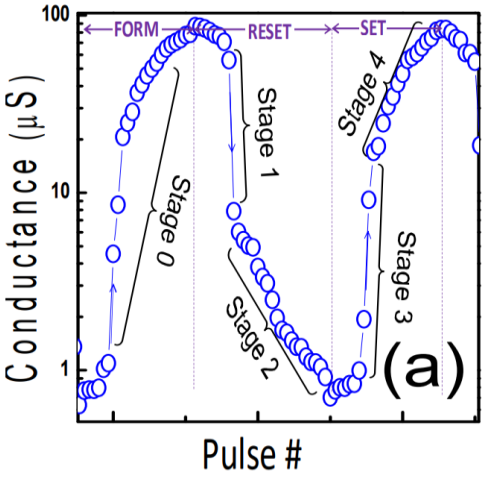
# Requirements

- Primary: Critical components for characterization
- Secondary: On chip programming, automated testing
- Tertiary: Higher risk structures for further testing

# Primary Requirements

- **Device Physics:**
  - Identify optimal voltages, pulse widths, # of pulses for operations
- **Endurance:**
  - Cycles to failure and resistance changes
- **Variability:**
  - Device-to-Device variation in silicon
- **Scalability:**
  - IR Drop when modules are combined




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# Secondary Requirements

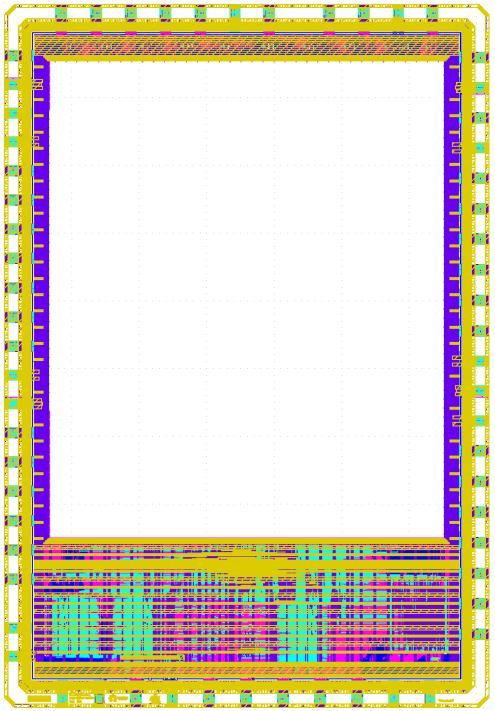
- **On-Chip Programming:**
  - Can ReRAM operations be done internally?
- **Automated Testing:**
  - Automated endurance
- **Multibit Mixed-Signal Blocks:**
  - DACs and ADCs for later compute

# Tertiary Requirements

- **Full Compute Crossbar:**
  - 2x2, 4x4 Full Crossbar
- **Neighboring Cell Effects:**
  - Reduce current sinking to adjacent columns
- **Thermal Device Interaction:**
  - On chip heater

# Hardware Constraints

- 2.92mm x 3.52 mm user area
- IO pin limitations
  - External parasitics
  - Internal logic analyzer
- Typical silicon constraints
  - 130nm PDK
  - Yields

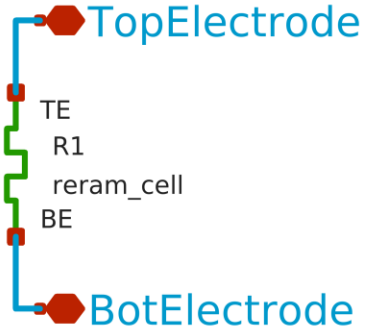


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# Software Constraints

- Open-source tools only
- Evolving documentation
- ReRAM spice model limited in functionality
  - No forming or Pex

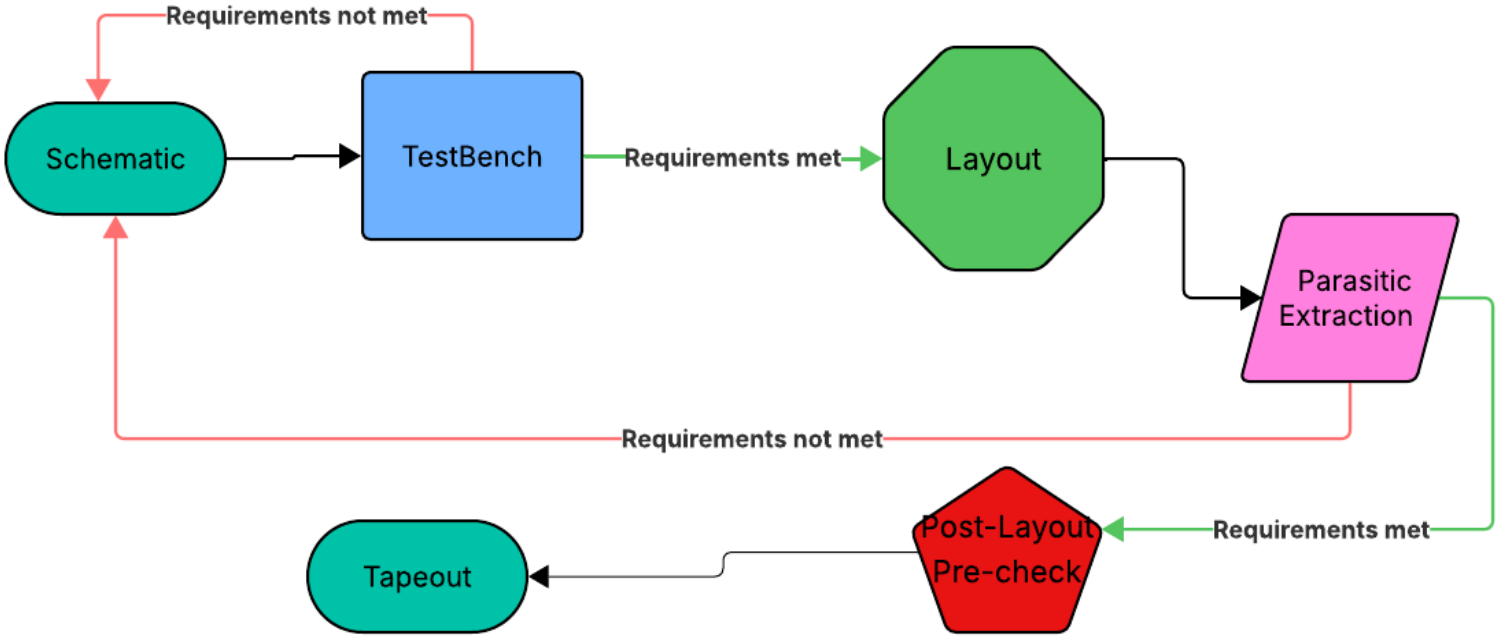




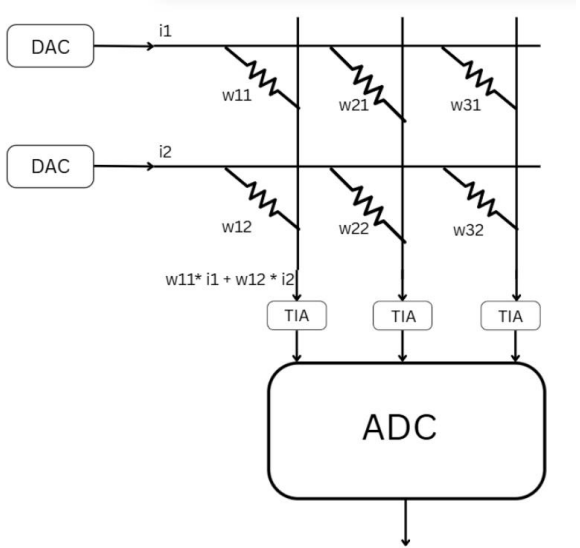

# Design

# Design Flowchart



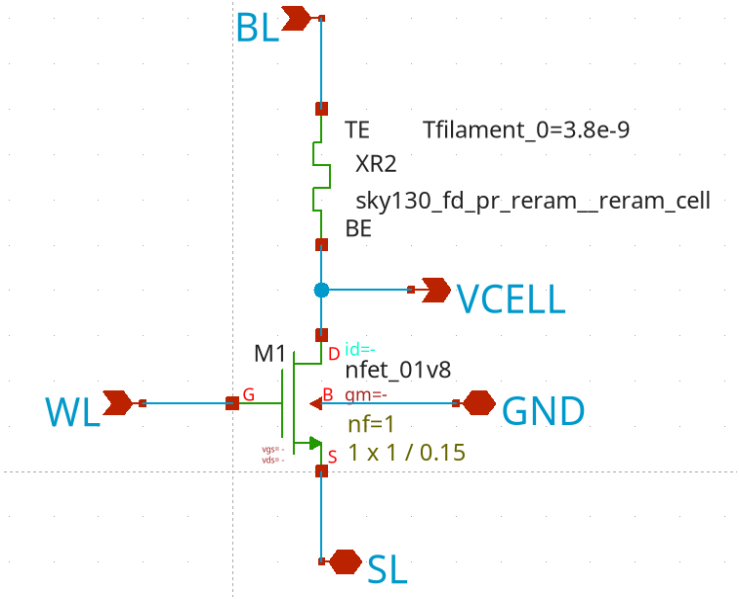
# High Level Full Design

- Use 1T1R as memristor modules
- The resulting voltage at the end at the TIAs is going to be the sum of the currents across the crossbar times the resistance down the crossbar.



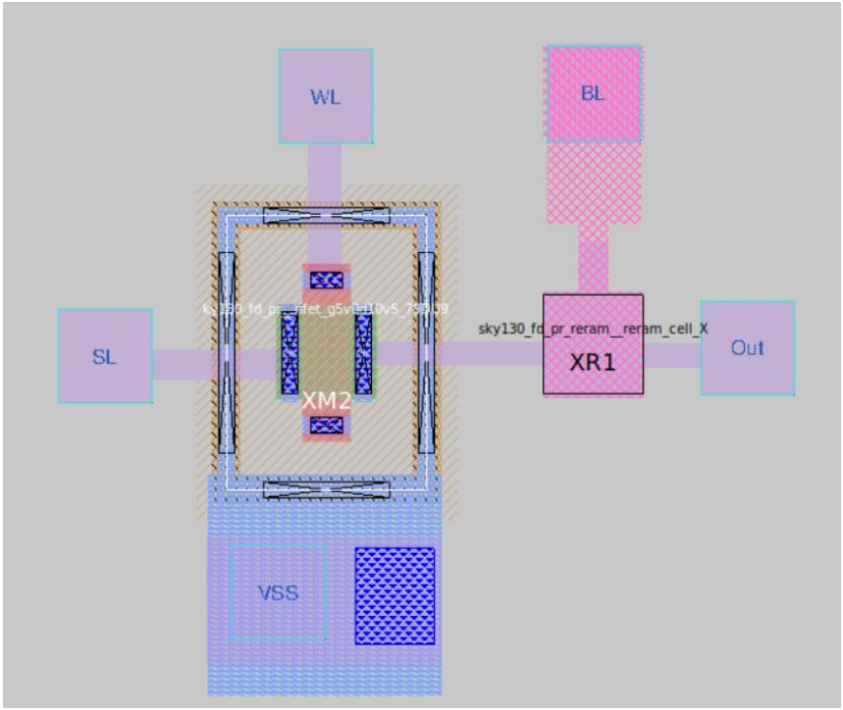
# 1T1R

- The 1T1R, 1 Transistor 1 Resistor (ReRAM), is the most fundamental module in the design of the ReRAM.
- The transistor acts as a gate that is activate through the Word-Line.
- This module can perform READ operations and WRITE operations.



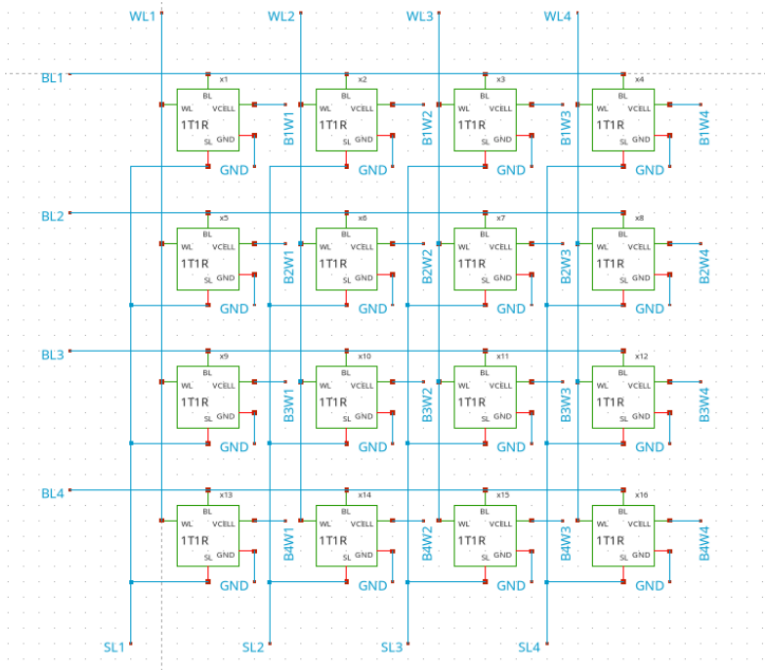

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# Layout 1T1R

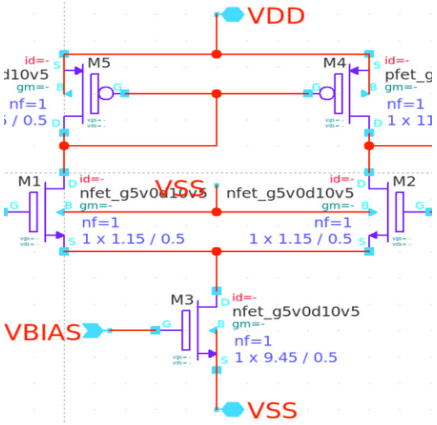


# 4X4 Crossbar

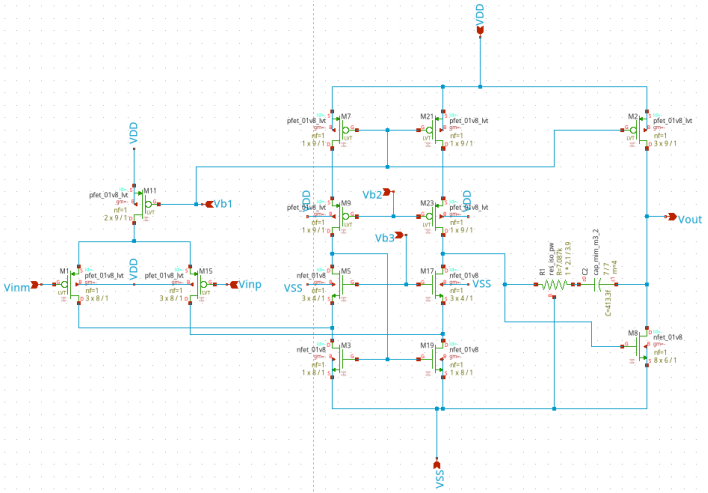
- Built using 1T1R modules
- This design simulates the implementation for a 4x4 matrix multiplication compute



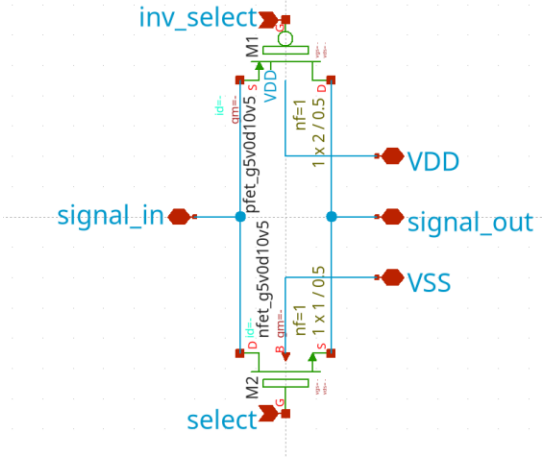
# More Designs




5T Op-amp



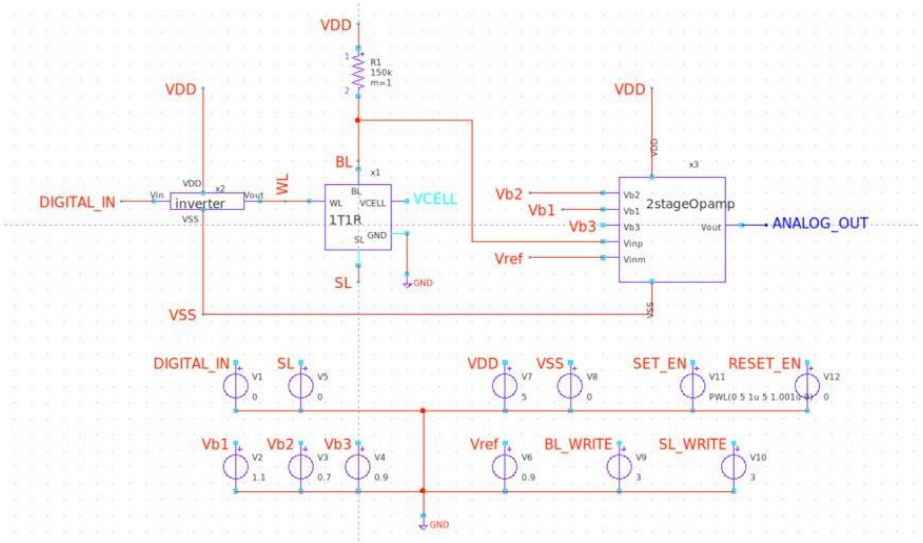

2 Stage Op-amp




Transmission Gate

# 1-Bit Full Compute Design

- Full 1-bit design ready for manufacturing
- Flow followed on a component-by-component basis
  - Inverter
  - 1T1R
  - TIA
  - ADC (Op-amp as Comparator)



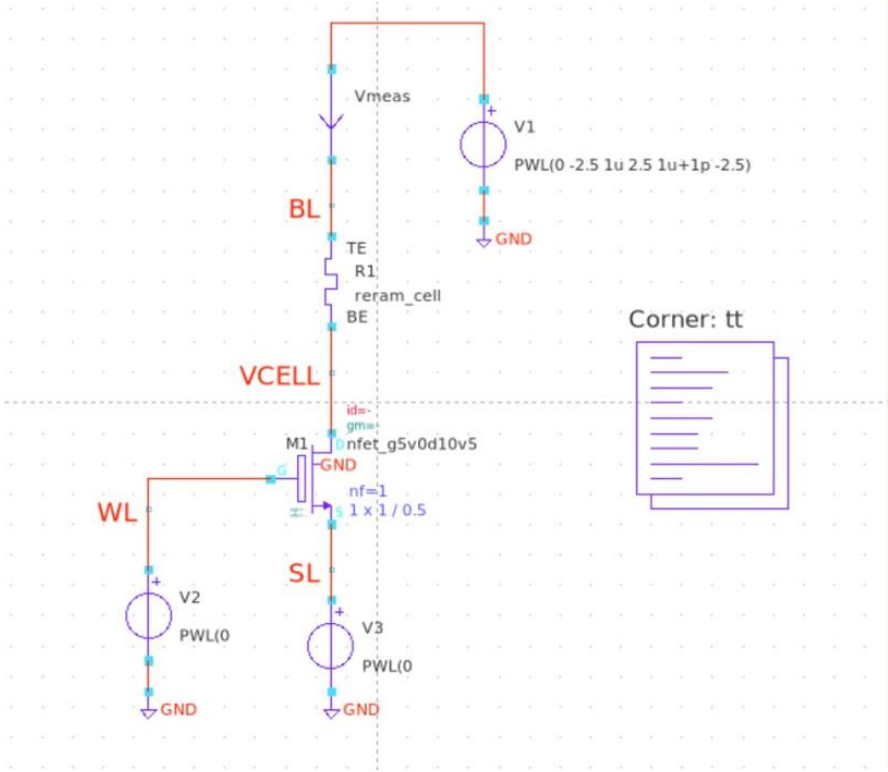
# Testing

# Test Procedure

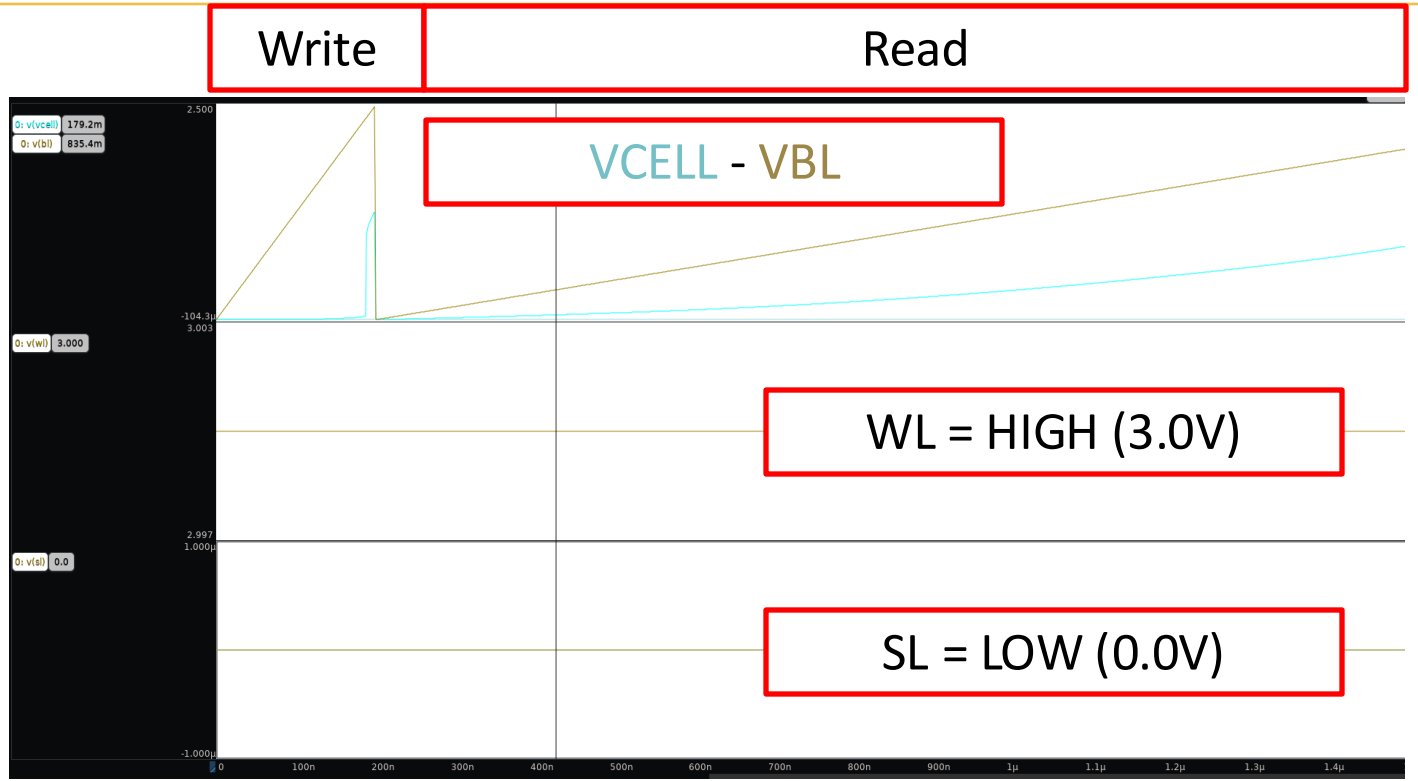
- Schematic design
- Simulations of testbench with ideal SPICE models
- Layout to extract parasitic capacitances and parasitic resistances through Magic VLSI
- Simulations with extracted models (not applicable to ReRAM)

# 1T1R Simulations

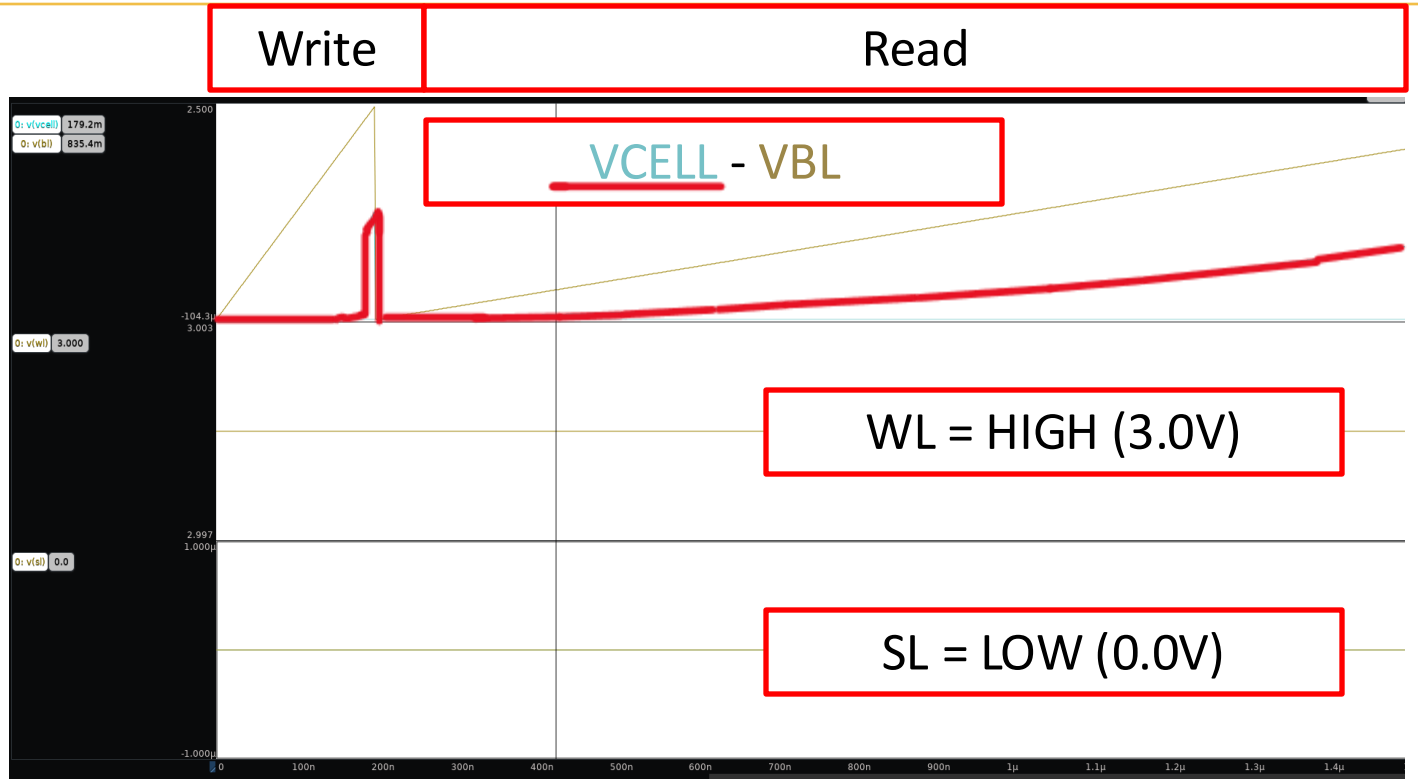
- Supports read/write with WL enable
- Writes are performed by passing a voltage through the ReRAM cell
  - SET > 2.4V (low resistance)
  - RESET < -1.8V (high resistance)
- READ observes the resistance state of the cell through BL (0V, 2.0V)



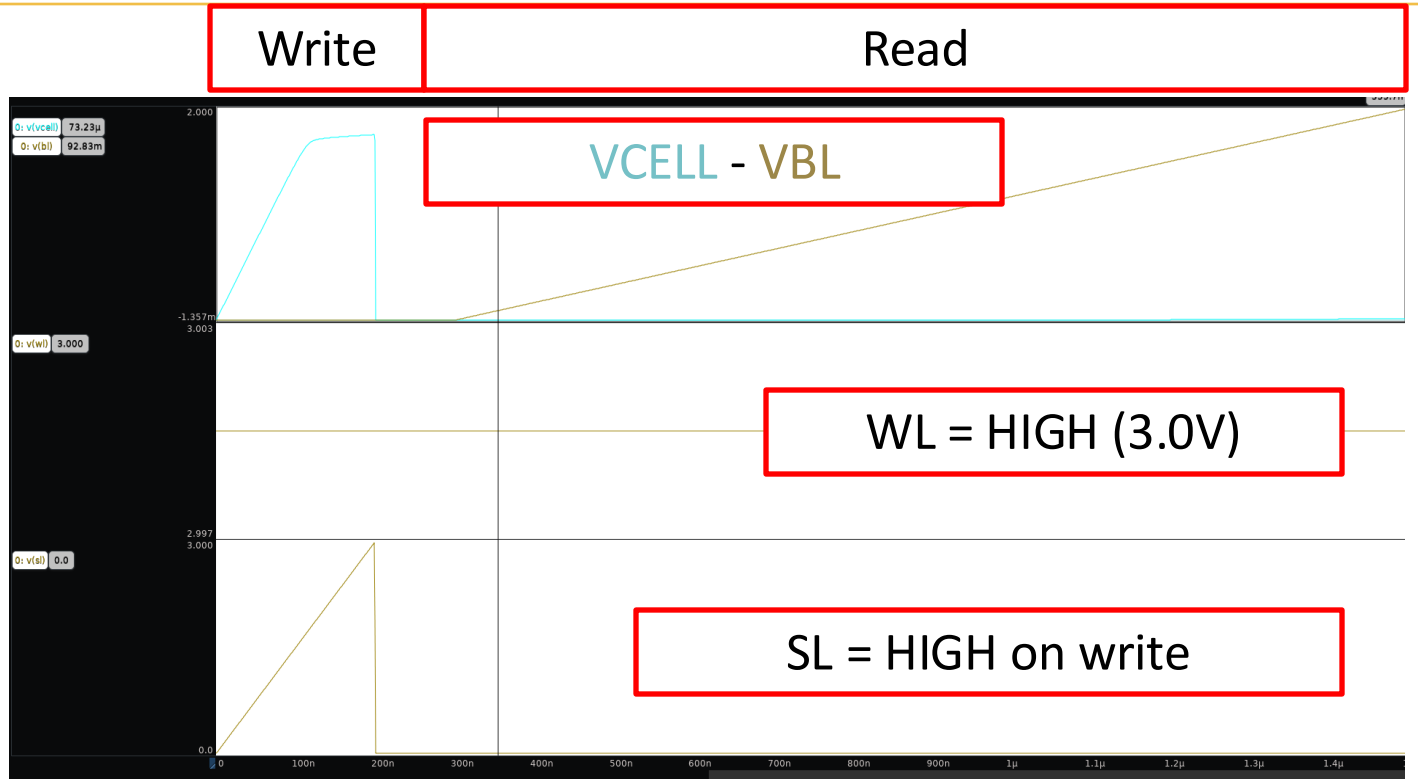
# 1T1R Results - SET



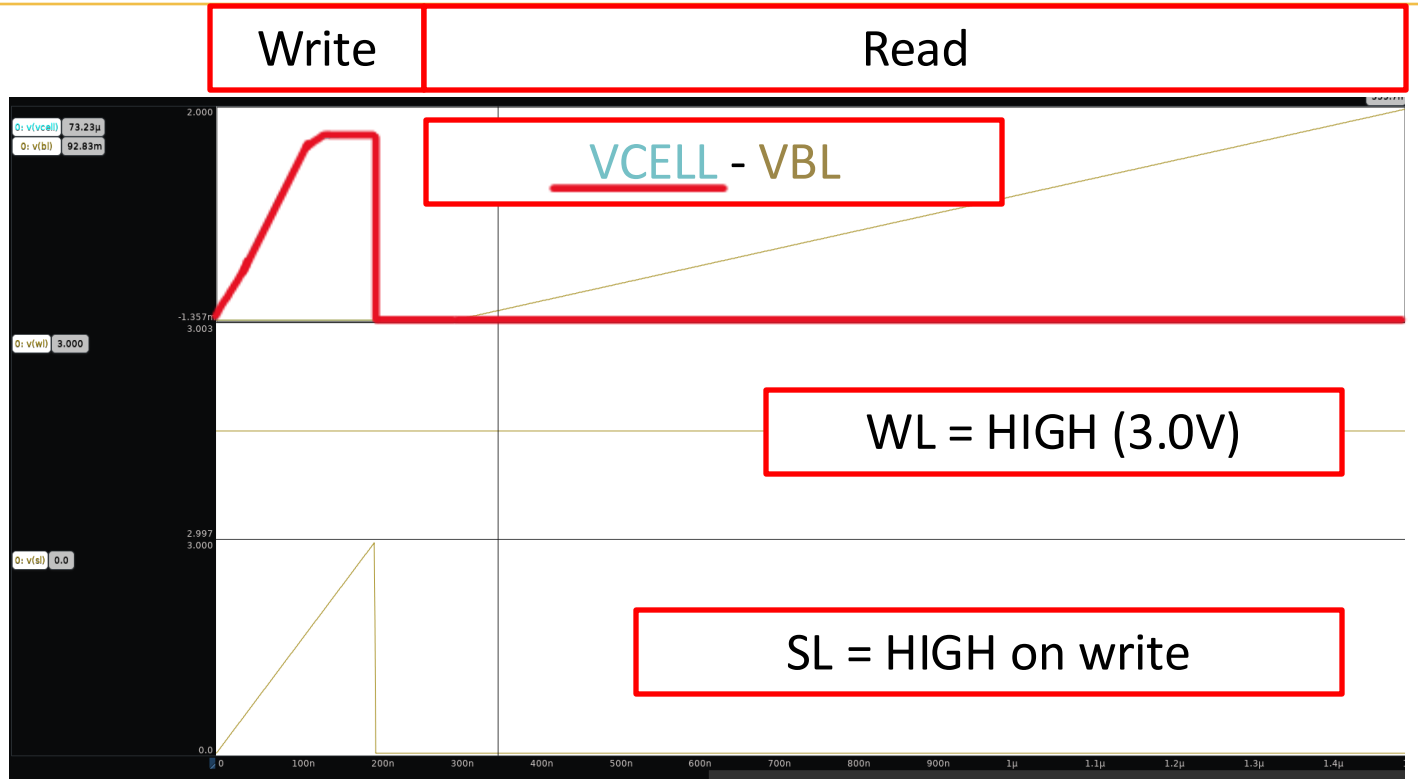
# 1T1R Results - SET



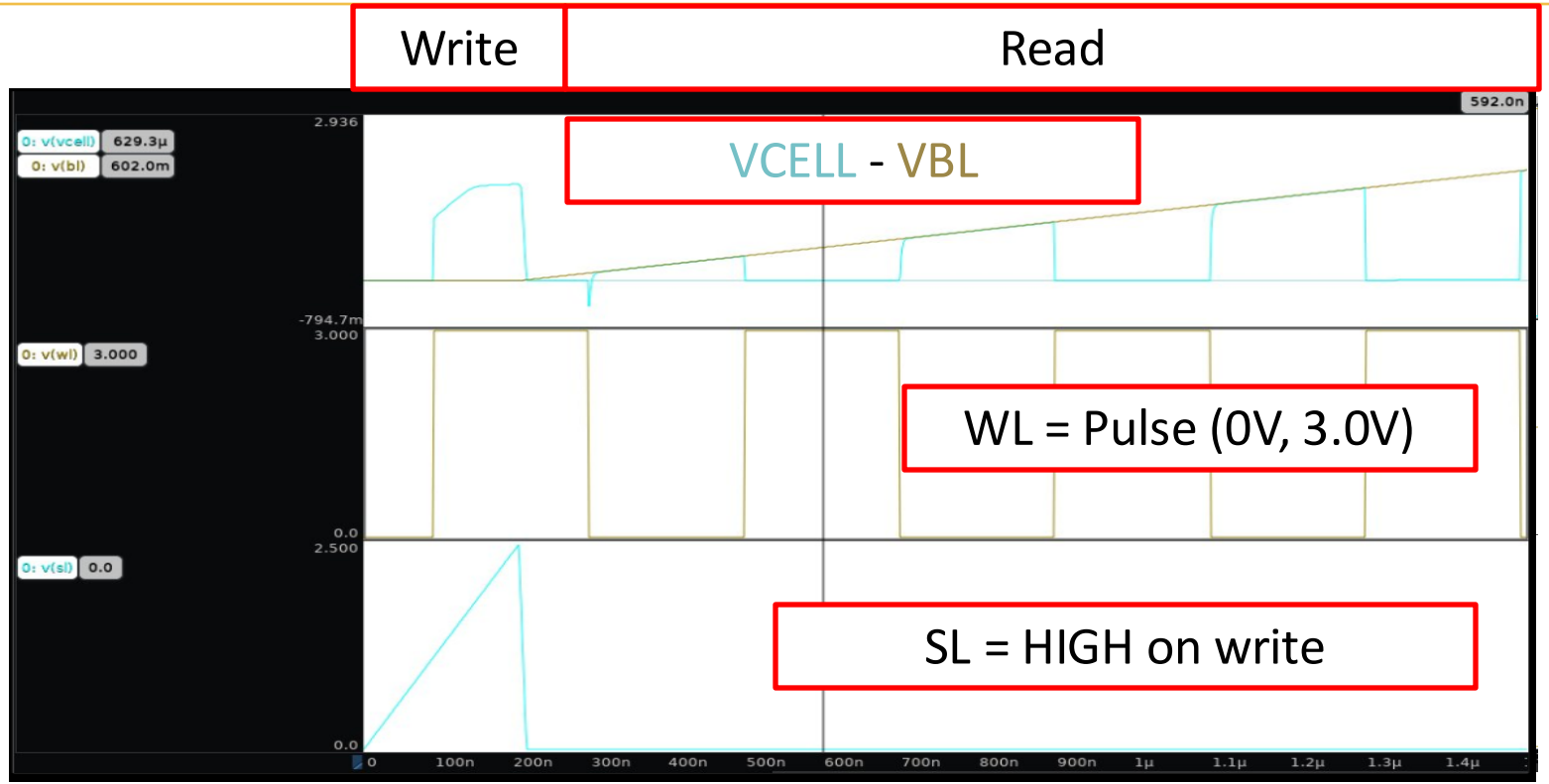
# 1T1R Results - RESET



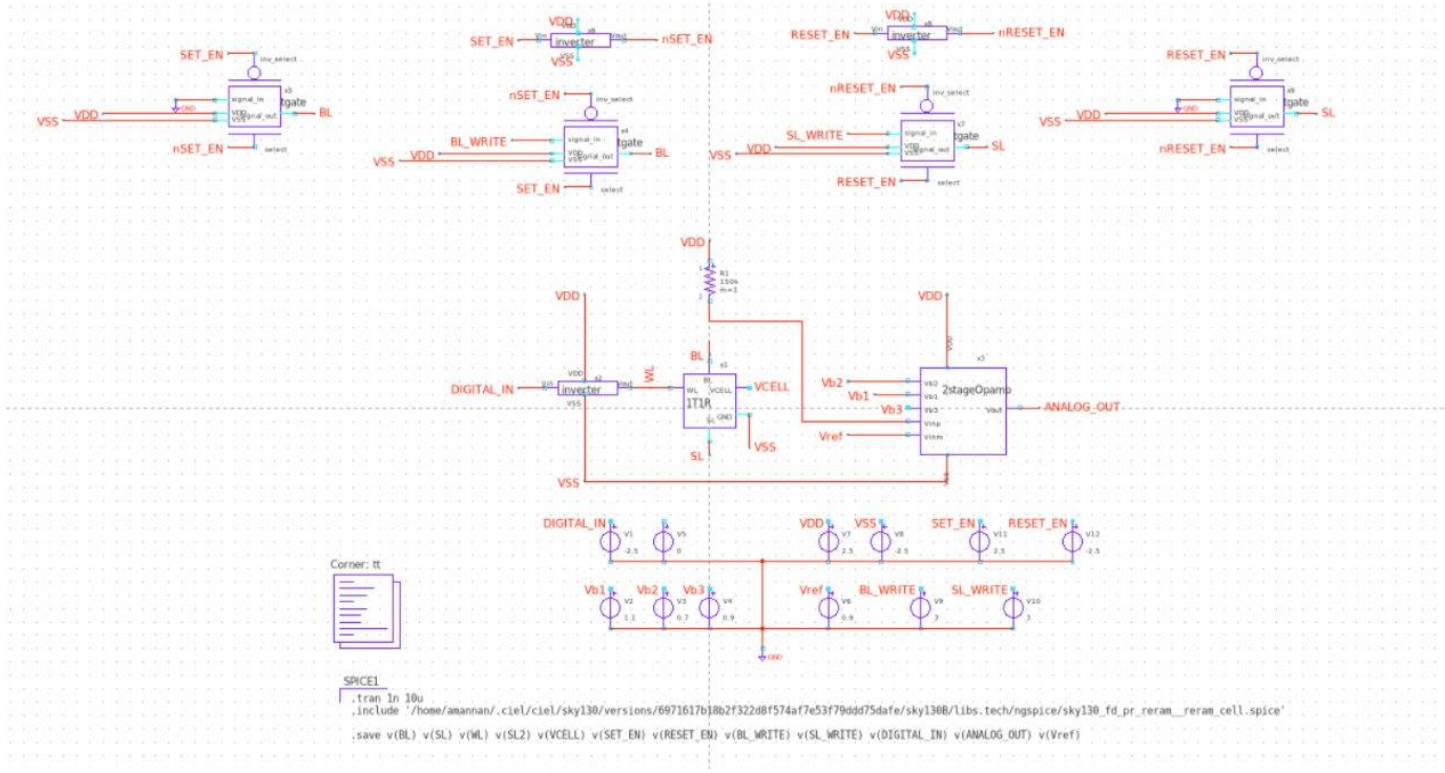
# 1T1R Results - RESET



# 1T1R Results – RESET with WL toggle



# Final Testbench for 1-bit Design



# What we are leaving for future teams

- This is a continuous project that has been going on for a few semesters now.
- The same way that last teams left some work for us to use we will leave something for the future teams.
- We created scripts that setup the open-source tools and PDK, so the next time can have an accelerated start
- All the components, testbenches and documentation that were made will be made available.

# Conclusion

- Designed and tested a 1-bit ReRAM compute design
- Designed components:
  - Operational Amplifier
  - Transmission Gate
  - Inverter
  - 1T1R
- Created scripts to help future teams have an accelerated start for future design and remove ambiguity on using design tools

# References

Slide 3 Image: Kim Y-S, Kwon M-W. Implementation of Boolean Logic Operations and Refresh Circuit for 2T DRAM-Based PIM Architecture. Electronics. 2025; 14(22):4483. https://doi.org/10.3390/electronics14224483

Slide 5 Image: Kim S, Lee J. TCAD Simulation of Resistive Switching Devices: Impact of ReRAM Configuration on Neuromorphic Computing. Nanomaterials. 2024; 14(23):1864. https://doi.org/10.3390/nano14231864

Slide 9: https://sky130-fd-pr-reram.readthedocs.io/en/latest/user_guide.html

Slide 12: https://chipfoundry.io/soc_platforms

# Thank you!

*Questions?*